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Digital Control Technologies for Modular DC-DC Converters

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Abstract— Recent trends in aerospace Power Management and Distribution (PMAD) systems focus on using commercial off-the-shelf (COTS) components as standard building blocks. This move to more modular designs has been driven by a desire to reduce costs and development times, but is also due to the impressive power density and efficiency numbers achieved by today's commercial DC-DC converters. However, the PMAD designer quickly learns of the hidden "costs" of using COTS converters. The most significant cost is the required addition of external input filters to meet strict electromagnetic interference (EMI) requirements for space systems. In fact, the high power density numbers achieved by the commercial manufacturers are greatly due to the lack of necessary input filters included in the COTS module. The NASA Glenn Research Center is currently pursuing a digital control technology that addresses this problem with modular DC-DC converters. This paper presents the digital control technologies that have been developed to greatly reduce the input filter requirements for paralleled, modular DC-DC converters. Initial test result show that the input filter's inductor size was reduced by 75%, and the capacitor size was reduced by 94% while maintaining the same power quality specifications.

1. INTRODUCTION

Current trends in Power Management and Distribution (PMAD) systems are focused on using modular "building block" components to meet the needs of specialized loads. While no modular system can ever match the performance of a custom built solution, modular components are nearing

the point where their negative system impacts are being greatly outweighed by their benefits.

The benefits of a truly modular PMAD system are many. Since modular components can be used in a variety of missions, the large quantity of modules manufactured decreases the price per module. In fact, several recent programs have used commercial off-the-shelf (COTS) components as building blocks to greatly reduce the cost of development. While less expensive components will lead to more affordable hardware, their cost is negligible when compared to the cost to develop custom hardware. The main benefit of modular designs is an almost complete elimination of the typical 12-24 month development times for custom hardware. The system design is simplified to selecting and integrating pre-engineered modules to meet the needs of the spacecraft, thereby reducing cost and compressing the schedule. Finally, in a modular design, the ability to add extra modules to achieve N+k redundancy improves system reliability.

These modular building blocks are, for the most part, commercial-off-the-shelf (COTS) DC-DC converters. We have seen an increasing number of spacecraft manufacturers rely on COTS converters to meet the power conversion requirements of their specialized loads. One recent example is a power supply built for a Hall effect thruster for the Express/T-160E spacecraft [1]. The Hall thruster required a regulated 300 Vdc, 15 A power source to be generated from a 50Vdc spacecraft bus. Instead of starting from scratch developing a specialized converter, the manufacturer turned to Vicor, Inc. (Andover, MA) to provide DC-DC converters as building blocks for the power processor.

Vicor has been very successful in the past several years in advancing the state-of-the-art in DC-DC converters. Their “2nd Generation” line of converters achieves very high power densities with impressive efficiencies. For example, their 2nd Generation Maxi converter is a 500 W converter and has a mass of only 220 grams, or a power density of over 2,200 W/kg. The efficiency is an equally impressive 89.5%. These numbers make the Vicor DC-DC converters very attractive to PMAD systems designers striving to reduce development times while still providing good system-level performance.

The design of the 300 Vdc converter used a combination of series and parallel converters to achieve the power levels necessary to drive the Hall thruster. The converter uses four paralleled strings, each made up of three 100 Vdc converters with series-connected outputs (Figure 1). Each string is capable of providing 5A or 1,500W at 100Vdc. The four strings available to provide the 4,500 W necessary to the load allowing one backup string in case of converter failure.

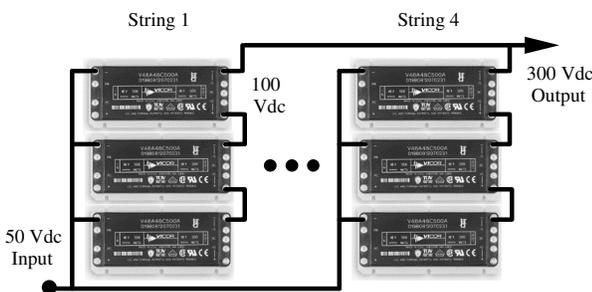


Figure 1 – Parallel/Series Configuration.

So far, the case for using COTS converters as modular building blocks seems to be faultless, until one starts to include the “add-ons” necessary for power quality, EMI, and control. Analysis of the design of the prototype power processor shows that the final power density achieved was only about 20% of the power density of the DC-DC converters; or 400 W/kg. One of the main causes for the loss of power density was the input filters required for power quality and EMI. These filters were as large as the DC-DC converters themselves, effectively halving their power density immediately (Figure 2).

It is clear that the use of modular DC-DC converters is the trend for future spacecraft. The benefits of low acquisition cost, fast development times, and simple redundancy implementations are the keys to affordable spacecraft and space missions. However, something must be done about the remaining negative effects of the large filters required for EMI and power quality specifications.

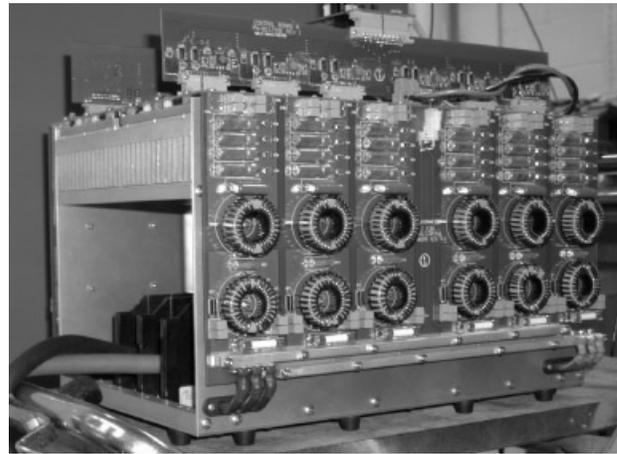


Figure 2 – Express/T-160E power processing unit prototype. Input filters shown.

2. PHASE SHIFT TECHNOLOGY DEVELOPMENT

An approach to input filter reduction that has been used in custom DC-DC converters in the past is the technique of phase shifting paralleled switch-mode power supplies (SMPS). By doing this, two benefits are accrued. First, the input current ripple magnitude is greatly reduced since the input currents cancel each other out when phase shifted properly. Second, the input current ripple frequency is increased resulting in a ripple frequency that is the baseline switching frequency multiplied by the number of SMPS in parallel. These two factors combine to significantly reduce the capacitive and inductive filtering which makes up a large part of all SMPS.

To investigate this technique, we first developed an analytical model to confirm our hypothesis. Our Electronics Workbench [3] model used two buck-converter models with the driving clock phase shifted 180° to the second unit. The resulting waveforms showed that this idealized system would have zero input current ripple. Although clearly the results of an idealized model, it confirmed our hypothesis.

Our next step was to validate the analytical model using actual hardware. Vicor DC-DC converters were readily available to us, having used them for many years in several technology development efforts and as spacecraft load simulators for our PMAD systems. The converters we used were the VI-200 series converters at 28 Vdc input and 5 Vdc outputs.

The Vicor converters use a zero current switching (ZCS) topology using an LC “tank” circuit. This converter topology is sometimes referred to as a quasi-resonant converter. With this topology, the inverter switch is turned on for a constant pulse width. Output regulation is achieved by changing the frequency that this fixed width pulse is applied to the switch [2]. A block diagram of the popular VI-200 series converter is shown in Figure 3. The switching

frequency varies from about 50kHz at low power to 400kHz at maximum load. The converters also provide synchronization inputs and outputs to allow paralleled converters to share power equally. Typically, one converter is designated as the “master”, providing the synchronization pulse to the “slave” converters. When the “master” and “slave” converters are all operating at the same frequency, power sharing is very good. In fact, Vicor produces both “master” and “slave” variations of the same converter. The slaves are exact copies of the master, but the output regulation circuitry has been removed to save on costs.

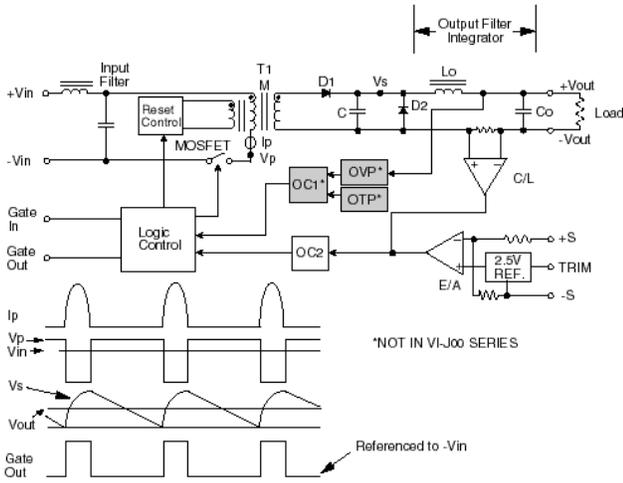


Figure 3 – Block Diagram of the Vicor™ VI-200 Series DC-DC Converter. [2]

Our goal was to intercept the synchronization pulse from the “master” to the “slave” and delay it by half the switching frequency (or 180°). A waveform generator was used to generate a delayed pulse triggered by the master synchronization pulse. By phase shifting the slave converter 180° we were able to reduce the input current ripple by a factor of three. At the same time, the ripple frequency was doubled. These two improvements have a great impact on the design of EMI filtering required for these DC-DC converters. A three-fold reduction in current ripple coupled with a doubling of ripple frequency will significantly reduce the input filter elements (inductors and capacitors) and thereby increase the power density of the resulting modular power converter.

Although this rudimentary test was limited to a fixed time delay and not a true phase shift, the positive test results encouraged further work. Our next effort was to develop and demonstrate a four-device modular power converter using a single microcontroller as the primary control element.

3. DIGITAL CONTROL RESEARCH

The modular power converter shown in Figure 4 uses four Vicor DC-DC converters connected in parallel. One converter is a master and the other three are slaves. The

master converter provides the regulation of the output voltage. The GATE OUT signal of the master is asserted when the master starts to draw current from the input bus. The slaves draw current from the bus when they are triggered by an assertion of their GATE IN input. There is no control of the pulse width since it is a fixed value determined by the resonant components in the DC-DC converter. Traditionally the slave converters are controlled by connecting the GATE OUT of the master directly to the slaves GATE IN terminal. Because of this the slave converters are all activated simultaneously and the input ripple current of the individual converters are in phase with each other. Our goal was to develop a digital controller that would phase shift the slave converters to reduce the input current ripple into the modular converter.

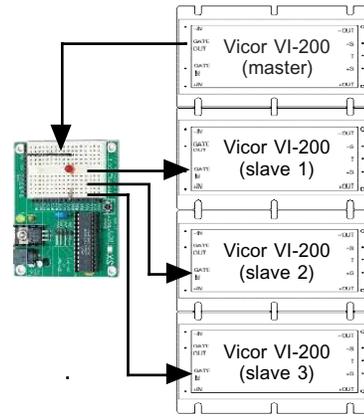


Figure 4 – Diagram of Vicor Phase Shift Test Setup

A Parallax SX-Key demo board using a Scenix SX28AC/DP microcontroller was used to provide the phase shift control of the four DC-DC converters [4]. The microcontroller was clocked at the maximum 50 MHz clock frequency. The Scenix microcontroller was programmed to accept the GATE OUT signal from the master converter as an input and generate three phase shifted signals for the slaves GATE IN inputs. The microcontroller was designed to delay the signal from the master to the individual slave converters in such a way as to minimize the input current ripple. For ideal waveforms, minimization of input current ripple occurs when,

$$d_k = \frac{k \cdot T}{n} \quad (1)$$

where d_k is the delay of the master’s signal to the k^{th} slave converter, T is the switching period, and n is the total number of active converters.

Phase Shift Control Algorithm

The microcontroller program was written in assembly language for the Scenix SX28AC/DP. The program consists of two elements: a main program loop and an interrupt routine. The main program loop is responsible for calculating the time period of the master GATE OUT signal,

monitoring the number of active converters, and calculating the slave converter's delay time based on equation (1).

Due to the extreme time sensitive nature of the pulse timings, a processor interrupt was used to stop the main program loop and enter the routine that generates the slave pulses. This interrupt routine is entered whenever the GATE OUT signal is asserted by the master converter. The interrupt routine's only purpose is to generate the delayed pulse signals to the slave converters based on the delay times calculated in the main loop. Once the interrupt routine is complete, the main program loop is resumed where it had left off.

Several interesting problems were encountered during the design of the controller software. First, the software was designed to be able to handle one master and up to three slaves. Simulated "power good" signals were generated from the active slave converters and polled occasionally by the microcontroller to determine the number of active slave units to be used in the delay time calculation. Note that in equation (1) that the time period, T, must be divided by the number of active units, n. This calculation is very simple for the case where there are 2 or 4 active units. The measured time period binary number is simply right-shifted once to divide by two and twice to divide by four. However, dividing by three required a little innovation.

Since the microcontroller has no DIVIDE function, we decided that we would have to approximate a division by three. With a little analysis it became clear that $X \cdot 0.333$ could be approximated using a series of subtractions using only right shifts of X to divide by the odd powers of two. Since X was limited to 8 bits, the closest we could get to one-third was the following equation:

$$\frac{X}{3} \cong \frac{X}{2} - \frac{X}{8} - \frac{X}{32} - \frac{X}{64} = 0.3281 \cdot X \quad (2)$$

Another limitation of the single microprocessor implementation is the fact that one processor had to output all three slave GATE IN signals. The interrupt routine which generates the delayed pulses must perform two functions. First, it must assert the first slave's GATE IN signal for a fixed amount of time and then un-assert the signal. It then must wait until it is time to assert the second slave's GATE IN signal. Consequently, the GATE IN signals for the slave converters cannot overlap and are limited to minimum delay times equal to the pulse width of the signal. Due to these factors, a maximum master converter frequency of only 133 kHz could be achieved when all four converters were active. This resulted in a maximum current output of only 11.5 A, or less than 25% of the total power capacity of the four paralleled units. In the future we hope to eliminate this limitation by using one microprocessor for each converter.

4. TEST RESULTS AND ANALYSES

Test results from the four converters operating in parallel with the microcontroller and without are presented below. The data shows the master GATE OUT signal on top with the three slave converter GATE IN signals beneath. Total input current into the four paralleled converters was measured using an AC coupled current probe. Figures 5 and 6 show the data with a very low load of only 3.1 A and Figures 7 and 8 show the same data with the maximum load of 11.5 A. The time scale of 5µs per division is constant for all figures as is the current ripple scale of 2.5 A per division.

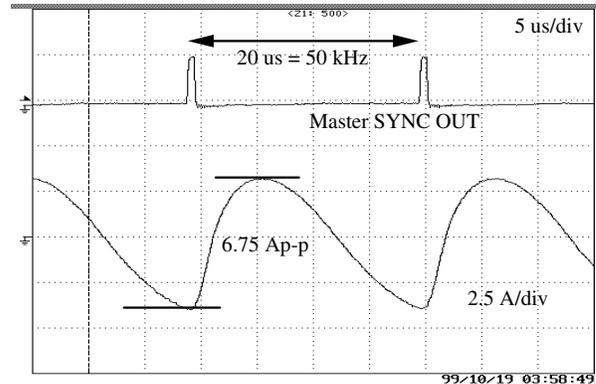


Figure 5 – Converters in-phase. Load = 3.1 A

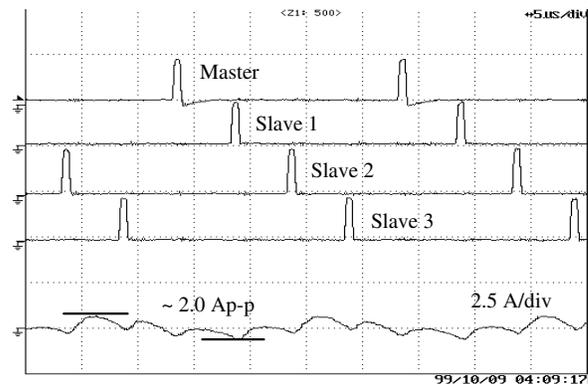


Figure 6 – Phase shifted converters. Load = 3.1 A

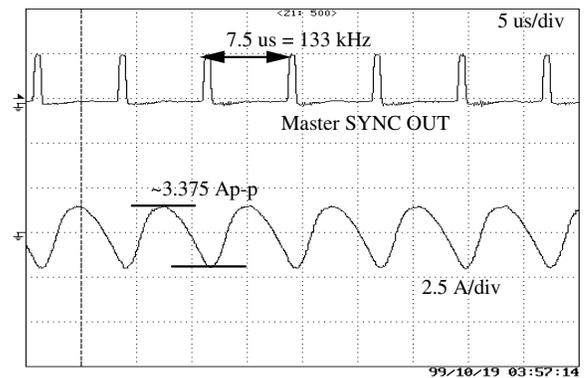


Figure 7 – Converters in phase. Load = 11.5 A

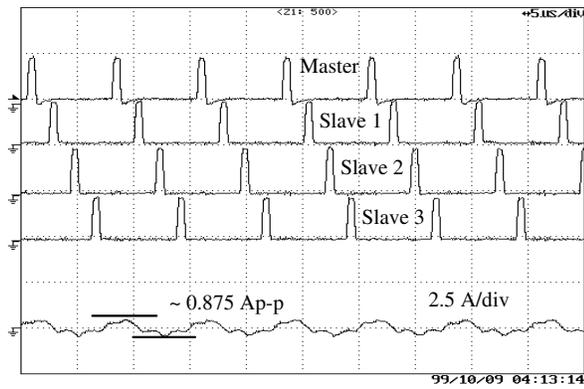


Figure 8 – Phase shifted converters. Load = 11.5 A

The significant improvements in input current ripple are clearly obvious. Also, Figure 8 demonstrates the limit of power processing as the slave pulses begin immediately following the completion of the previous pulse as described above.

Matlab was used to analyze the frequency spectrum of the input current ripple. The frequency components were calculated using a fast Fourier transform (FFT) algorithm on time domain data obtained from the digital oscilloscope. The results for the phase shifted and in-phase configurations, with a 3.1 A load, can be seen in Figure 9 and Figure 10 respectively. The amplitude of the first harmonic is seen to be 3.1 A when the converters are connected in phase. However the amplitude of the first harmonic is reduced to 0.45 A with the phase shifting program running.

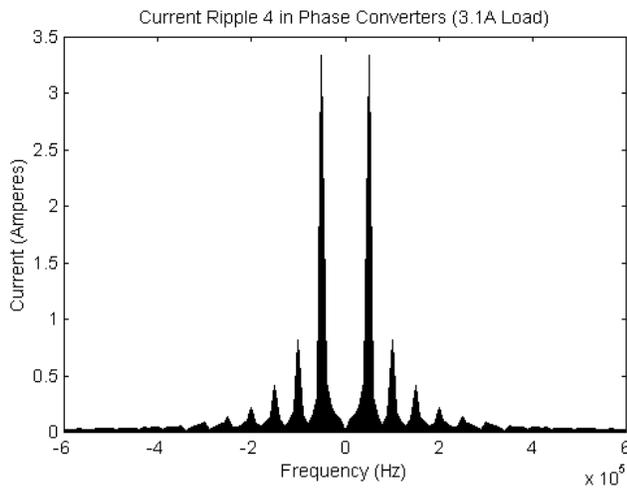


Figure 9 – Spectrum of input current (in-phase, 3.1A)

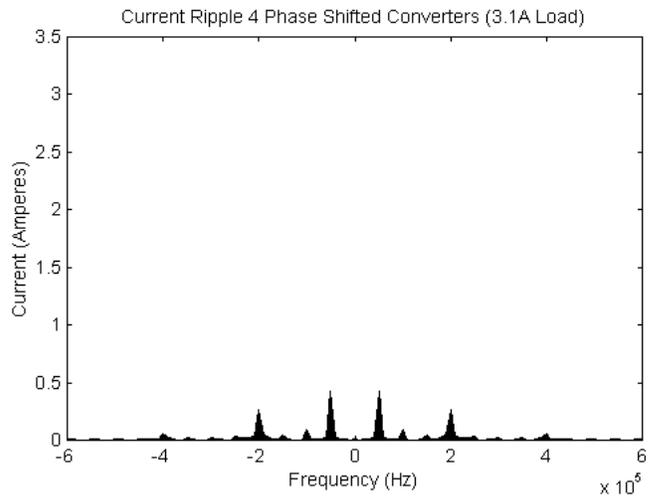


Figure 10 – Spectrum of input current (phase shift, 3.1A)

The frequency results with an 11.5 A load for the in phase and phase shifted configurations are shown in Figure 11 and Figure 12 respectively. The amplitude of the first harmonic is seen to be 1.5 A for the in phase configuration, while the phase shifted configuration has a first harmonic amplitude of only 0.3 A. It is interesting to note that all of the other harmonics are greatly attenuated compared to 4th harmonics in the phase shifting configuration. This is as expected because there are four converters running in parallel. Theoretically if all of the converters produced identical current waveforms there would be no harmonic component at the fundamental frequency of the master converter. However because of slight differences in these current waveforms there is still a significant residual component at this frequency.

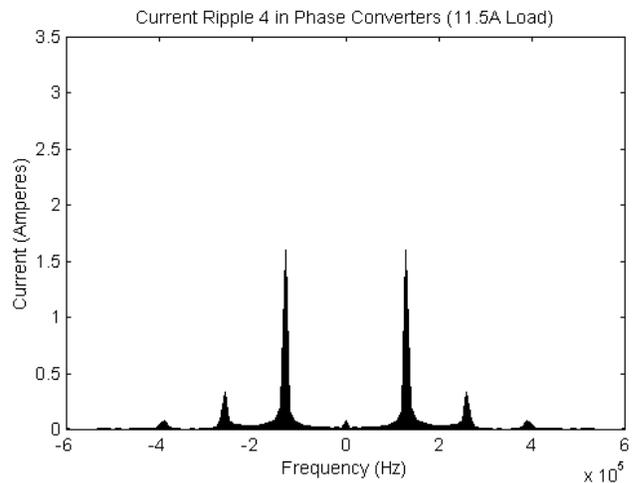


Figure 11 – Spectrum of input current (in-phase, 11.5A)

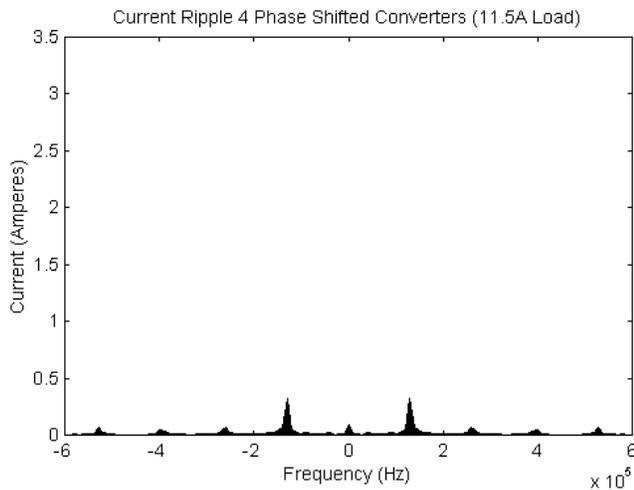


Figure 12 – Spectrum of input current (phase shift, 11.5A)

A further concern was to find out how well the DC-DC converters shared power in this configuration. To test this, current probes were placed on the inputs of the individual DC-DC converters. Current data for each of the four converters was obtained for load conditions of 3.1 A and 11.5 A. This data was then converted to instantaneous power in Matlab by multiplying the current waveform data by the input voltage waveform on the input bus. The average of these instantaneous power waveforms was then calculated in Matlab. The results can be seen in Figure 13 and Figure 14 for loads of 3.1 A and 11.5 A respectively. With a load of 3.1 A, the converters share power within 6.5% of each other. At an 11.5 A load, the converters share power within 2.2% of each other.

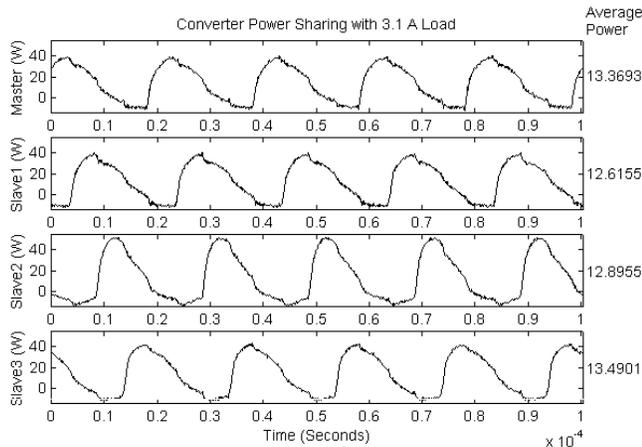


Figure 13 – Instantaneous power waveforms (3.1 A)

To demonstrate the benefits of the phase shifting technique, an example filter was designed for both the phase-shifted and in-phase configuration. The specifications used for the

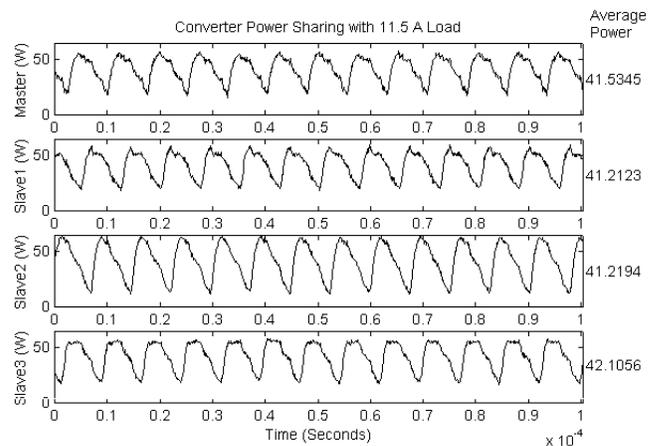


Figure 14 – Instantaneous power waveforms (11.5 A)

example filter are a maximum current ripple of 100 mA and a maximum voltage ripple of 5% of the input voltage (1.2 V). The data from the 11.5 A load given above will be used for the analysis. The in-phase configuration will be studied first. The peak-to-peak current, at an 11.5 A load, was found to be 3.375 A at 133 kHz. The filter configuration is simply a series inductor and shunt capacitor. Consider the equation for capacitor current,

$$i_c = C \cdot \frac{dv}{dt} \quad (3)$$

This can be rewritten as,

$$C = i_c \cdot \frac{dt}{dv} \quad (4)$$

It is known, from the specification, that the inductor should carry only 100 mA, thus the capacitor current is given by,

$$i_c = (3.375 - 0.1) \text{ A} = 3.275 \text{ A}$$

As a worst case estimate the switching duty cycle is assumed to be 0.5, thus

$$dt = \frac{T_s}{2} \quad (5)$$

Where T_s is the switching period, namely

$$T_s = \frac{1}{F_s} \quad (6)$$

From the specification it is known that $dv = 1.2 \text{ V}$, thus the capacitance is calculated with equation (4) to be 10.26 μF . The series inductor can then be calculated from the following,

$$V_L = L \cdot \frac{di}{dt} \quad (7)$$

This can be rewritten as,

$$L = V_L \cdot \frac{dt}{di} \quad (8)$$

Where the voltage across the inductor, V_L , is simply equal to the ripple voltage or 1.2 V. Further to meet the specification it is necessary that, $di = 100\text{mA}$. Thus it is seen from equation (8) that the inductance is 45.11 μH .

For the phase shifted configuration, a peak-to-peak ripple current of 0.875 A with a frequency of 532 kHz (4 x 133 kHz) was observed. Using the same reasoning that was applied for the in phase case, it is seen that $C=0.607 \mu\text{F}$ and $L=11.28 \mu\text{H}$. Thus the phase shifting technique lowers the required inductance by a factor of 4 and the required capacitance by a factor of 16.

	Baseline	Phase shift	Reduction
Capacitance (μF)	10.26	0.61	94%
Inductance (μH)	45.11	11.28	75%

Table 1 – Reduction in Input Filter Size

5. FUTURE WORK

While the results obtained so far are very promising, there are several areas we will be investigating in the very near future. The first area of interest is to determine why the phase shift technique was not completely successful in eliminating the fundamental frequency component of the master converter. With ideal, phase shifted converters, one would expect a complete elimination of the fundamental frequency. However, looking at the instantaneous power waveforms, it is clear that not all converters exhibited the same input current waveform shape. This may have led to the unexpected results. We plan to continue testing to determine if the cause is due to the non-symmetric waveforms, or possibly that the optimum phase shift angle may not be 90° for all or some of the converters.

Second, we'll be looking at other converter topologies and synchronization methods to evaluate the applicability of this technology to other manufacturer's converters. These include the Vicor 2nd Generation DC-DC converter modules and, more importantly, fixed frequency DC-DC converters from Interpoint and other manufacturers.

Other plans call for further development of the phase shift technology to the point where it can be incorporated into the

design of the DC-DC converter. This includes looking into the possibility of using analog controllers and an extension of the digital controller development using a microprocessor for each converter. These implementations would eliminate the limitations on switching frequency that are caused by the inability of the slave signals to overlap.

For the multiple microcontroller implementation, we envision each controller having three modes of operation. These modes will depend on the state of the DC-DC converter they are controlling. In particular there will be a mode for master, slave, and power bad. The master mode will calculate the delay based on the number of active converters and the period of the master's gate out signal. The number of active converters would be detected by polling the other microcontrollers with a communication bus. This delay would be transmitted to the other microcontrollers over a communication bus. The master mode microcontroller would pass the master's gate out signal with no delay to the next microcontroller. A slave mode microcontroller would simply delay the gate signal received from the previous microcontroller and then output the signal to both the slave converter, which it is controlling, and to the next microcontroller. In the power bad mode, the gate signal of the previous microcontroller would be simply passed to the next converter. This allows a converter to be bypassed if it fails to operate properly.

Finally, we will be developing digital control strategies that could allow for distributed converters to operate in parallel with no external synchronization or communication. This would require digital signal processing algorithms to be included in each converter to detect system bus noise profiles and phases that could then be used to minimize overall system noise.

6. CONCLUSIONS

It is clear that current trends to include more commercial components in spacecraft hardware is not likely to reverse in the near future. It is therefore important to make sure that system performance metrics of power density and efficiency are not greatly sacrificed for the economic reasons of cost and time. Our initial research into using phase shift techniques to reduce the filter size required for commercial DC-DC converters has proved very promising. Using a small, inexpensive microcontroller, we were able to significantly reduce the input current ripple generated by four DC-DC converters connected in parallel. The result is that the input filter's inductor size was reduced by 75%, and the capacitor size was reduced by 94%. It is clear that this technology will be an important component in reducing the size of modular power systems in the future.

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- [4] Parallax, Inc., 599 Menlo Drive, Suite #100, Rocklin, CA 95765, 888–512–1024, <http://www.parallaxinc.com>

8. BIOGRAPHY



Mr. Robert M. Button has been working at the NASA Glenn (Lewis) Research Center since 1987. He has a BSEE from Carnegie Mellon University, 1987 and an MSEE from Cleveland State University, 1989. He was the lead engineer of the Space Station Freedom source subsystem in the Power Management and Distribution Test Bed at the NASA Lewis from 1989-1994. He conducted specialized tests including the evaluation of a peak power tracking method and impedance testing of an 82 cell NiH₂ engineering model battery for the Space Station Freedom. From 1994-1998 he led the development and testing of the Series Connected Boost Regulator (SCBR) technology as applied to solar array and battery charge regulation. Currently he is leading the Power Management and Distribution Advanced Technology Element at NASA Glenn which is focused on the development of digital controller technologies in modular power systems.



Mr. Peter E. Kascak received his BSEE and MSEE from The Ohio State University in 1997 and 1999. From 1997 to 1999 he was a member of the Analog Very Large Scale Integration (VLSI) Laboratory at The Ohio State University. From 1996 to 1998 he worked as a summer intern at NASA Glenn (Lewis) Research Center in Cleveland Ohio. He developed a microcontroller-based motor controller to control the opening and closing of a flight-qualified switch for the International Space Station. He is currently working full time at NASA Glenn as a senior research associate for the Ohio Aerospace Institute (OAI).



Mr. Ramon C. Lebron-Velilla obtained his BSEE degree from the University of Puerto Rico, Mayaguez Campus in 1990 and his MSEE degree from Cleveland State University in 1994. In 1990, he joined NASA Glenn (Lewis) Research Center in Cleveland, Ohio as an Electrical Engineer responsible for testing, evaluation, and verification of advanced development Space Station Freedom power system components for the Power Management and Distribution (PMAD) DC Test Bed. In 1995, Mr. Lebron was responsible for the design, development, test, and integration of the in-house power technology demonstration flight experiment PRKE (Photovoltaic Regulator Kit Experiment) for the Small Spacecraft Technology Initiative satellite. Presently, Mr. Lebron is responsible for the development, test, and integration of the Electric Power Control Unit (EPCU) for the International Space Station Fluids and Combustion Facility. In addition, he is involved in the design, development, and testing of advanced high voltage distribution switchgear for space applications. Mr. Lebron is a registered Professional Engineer (P.E.) in the state of Ohio.

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13. ABSTRACT (Maximum 200 words) Recent trends in aerospace Power Management and Distribution (PMAD) systems focus on using commercial off-the-shelf (COTS) components as standard building blocks. This move to more modular designs has been driven by a desire to reduce costs and development times, but is also due to the impressive power density and efficiency numbers achieved by today's commercial DC-DC converters. However, the PMAD designer quickly learns of the hidden "costs" of using COTS converters. The most significant cost is the required addition of external input filters to meet strict electromagnetic interference (EMI) requirements for space systems. In fact, the high power density numbers achieved by the commercial manufacturers are greatly due to the lack of necessary input filters included in the COTS module. The NASA Glenn Research Center is currently pursuing a digital control technology that addresses this problem with modular DC-DC converters. This paper presents the digital control technologies that have been developed to greatly reduce the input filter requirements for paralleled, modular DC-DC converters. Initial test result show that the input filter's inductor size was reduced by 75 percent, and the capacitor size was reduced by 94 percent while maintaining the same power quality specifications.				
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